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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/745,969	12/21/2000	Qiang Wu	4239010689	8506

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EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2634	4

DATE MAILED: 03/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/745,969	Applicant(s) WU ET AL	
	Examiner Jason M Perilla	Art Unit 2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,15-17 and 19* is/are rejected.

7)☒ Claim(s) *3,5-14,18 and 20-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 are pending in the instant application.

Claim Rejections - 35 USC § 102

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1, 15, and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Zhang (6038435).

Regarding claim 1, Zhang discloses by figure 2 a digital signal processor comprising: an analog front end (4 and 5) including an analog-to-digital converter (5) for receiving an input signal; a digital base-band processor (fig. 1, refs. 12-14; fig. 2, ref. 41; col. 2, lines 60-65) having a latency period for detecting a signal (inherent), coupled to the analog front end; a shift register (22) for tracking data representing the relative amplitude of samples of the input signal; a gain control counter (31 and 28) controlled by a current relative amplitude of sample of the input signal (18) and an output from the shift register (22), coupled to the shift register; and a gain control circuit (32 and 3) coupled to the counter for controlling gain of the input signal. It is inherent that a latency

is present between the analog front end (AFE) and the base-band processor (DSP). The shift register is used to track data representing the relative amplitude of samples of the input signal (col. 3, line 57 – col. 4, line 15; col. 5, line 48 – col. 6, line 15). The gain control counter (31) is controlled by an output of the shift register (39) being coupled to the shift register (22), and a current relative amplitude of sample of the input signal (18 and 20). The current relative sample of the input symbol is applied to the shift register from the error accumulator (18) which is divided by the number of symbols (counter – 20) above the upper threshold (17). Hence, the gain control counter is controlled by a current relative amplitude of sample (accumulation of error divided by the number of symbols) of the input signal.

Regarding claim 15, Zhang discloses a digital signal processor (fig. 1, refs. 12-14; fig. 2, ref. 41; col. 2, lines 60-65) having a latency period (inherent) for detecting a signal, an improvement comprising: memory means for recording a history of the relative amplitude of samples of an input to the processor (fig. 2, refs. 18, 22, and 31); and gain control means (3) for controlling the gain of the input to the processor based upon the current amplitude of the input to the processor (22) and the relative amplitude of prior input samples recorded in the memory means (31). The gain control means stores currently the relative amplitude of prior input samples in the gain control counter (31) and also alters the gain control means by the current amplitude of the input to the processor (22) (col. 3, line 57 – col. 4, line 15; col. 5, line 48 – col. 6, line 15).

Regarding claim 19, Zhang discloses by figure 2 a method for controlling gain in a digital signal processor comprising: tracking data representing the relative amplitude

of an input signal (22); and controlling the gain by considering a current amplitude (38) and a prior amplitude (18) from the tracked data (col. 3, line 57 – col. 4, line 15; col. 5, line 48 – col. 6, line 15).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 4, 16, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang.

Regarding claim 2, Zhang discloses the limitations of claim 1 as applied above. Further, Zhang discloses that the digital signal processor wherein the shift register tracks data continuously (col. 4, lines 43-48). Therefore it would have been obvious to one of ordinary skill in the art at the time which the invention was made that the shift register of Zhang would track data representing a period equal to at least the latency period. Zhang discloses that the samples are taken over a sample window (col. 6, lines 32-36), and it would have been obvious to one of ordinary skill in the art that the period of the sample window would have been at least as long as the latency period of signal detection by the DSP.

Regarding claim 4, Zhang discloses the limitations of claim 2 as applied above. Further, Zhang discloses by figure 2 that the gain control circuit includes a comparator (27) for comparing a count in the gain control counter (28) with a predetermined count

(36) and based upon the results of the comparison, adjusts the gain of the input signal (col. 6, lines 25-37).

Regarding claim 16, Zhang discloses the limitations of claim 15 as applied above. Further, Zhang discloses that the digital signal processor wherein the memory tracks data continuously (col. 4, lines 43-48). Therefore it would have been obvious to one of ordinary skill in the art at the time which the invention was made that the memory register of Zhang would track data representing a period equal to at least the latency period. Zhang discloses that the samples are taken over a sample window (col. 6, lines 32-36), and it would have been obvious to one of ordinary skill in the art that the period of the sample window memory would have been at least as long as the latency period of signal detection by the DSP.

Regarding claim 17, Zhang discloses the limitations of claim 16 as applied above. Further, one skilled in the art understands that a shift register is comprised of a plurality of shift register stages. Hence, the shift register of Zhang comprises at least a first and a second shift register.

Allowable Subject Matter

5. Claims 3, 5, 6-14, 18, and 20-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art references not relied upon above are cited to further show the state of the art with respect to automatic gain correction circuits.

U.S. Pat. No. 6418303 to Blackburn et al; Fast Attack AGC circuit.

U.S. Pat. No. 5134631 to Kingston et al; Digital Gain controller.

U.S. Pat. No. 6094481 to Deville et al; Telephone with AGC.

U.S. Pat. No. 4075573 to Kennedy et al; AGC with controllable increments.

U.S. Pat. No. 6148046 to Hussein et al; Blind AGC system.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M Perilla whose telephone number is (703) 305-0374. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Chin can be reached on (703) 305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M Perilla
February 19, 2004

jmp

STEPHEN CHIN
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